

High Intercept Low Noise Amplifier for 1.9 GHz PCS and 2.1 GHz W-CDMA Applications using the ATF-55143 Enhancement Mode PHEMT

Application Note 1241

Introduction

Agilent Technologies' ATF-55143 is a low noise enhancement mode PHEMT designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. Agilent Technologies' new enhancement mode technology provides superior performance while allowing a dc grounded source amplifier with a single polarity power supply to be easily designed and built. Unlike a typical depletion mode PHEMT where the gate must be made negative with respect to the source for proper operation, an enhancement mode PHEMT requires that the gate be made more positive than the source for normal operation. Biasing an enhancement mode PHEMT is much like biasing the typical bipolar junction transistor. Instead of a 0.7 V base to emitter voltage, the ATF-55143 enhancement mode PHEMT requires about a 0.45 V potential between the gate and source for nominal 10 mA drain current.

The ATF-55143 is housed in a 4-lead SC-70 (SOT-343) surface mount plastic package. The 400 micron gate width of the ATF-55143 makes it ideal for applications in the 2 to 10 GHz frequency range by providing low noise figure coincident with high intercept point.

This application note describes the use of the ATF-55143 in a low noise amplifier optimized for the 1930 to 1990 MHz band for PCS handset station applications. The amplifier also provides very good performance for 2.1 GHz W-CDMA applications. The amplifier design combines low noise figure and good third order intercept point (IP₃) while maintaining good input and output return loss. The amplifier makes use of surface mount miniature multi-layer chip inductors for a compact layout.

The LNA is designed for a nominal power supply voltage V_{dd} of 3 V. When biased at a bias point of V_{ds} = 2.7 V and I_d of 10 mA, the ATF-55143 amplifier provides a nominal 0.8 to 0.9 dB noise figure with a typical gain of 15 to 16 dB at 1960 MHz. Output intercept point (OIP₃) is measured at a nominal +21.6 dBm making the device capable of a nominal input intercept point (IIP₃) of +5.3 dBm.

LNA Demo Board

For applications up through 2.4 GHz, a generic demonstration board was developed. The board as shown in Figure 1 is etched on 0.031" FR-4 for low cost. The board utilizes small surface mount components. Input and output connectors are via E.F. Johnson SMA connectors part number 142-0701-881.

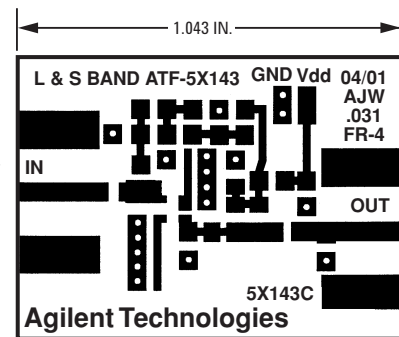


Figure 1. Artwork for the ATF-55143 Low Noise Amplifier Demonstration Board. Actual dimensions 1.043" by 0.755".

PCS Amplifier Design

The schematic diagram describing the PCS low noise amplifier is shown in Figure 2. Circuit topology is very similar to the typical depletion mode circuit except for the method of biasing the device. A parts placement drawing is shown in Figure 3. The parts list for the amplifier is shown in Table 1. A picture of a completed demonstration board is shown in Figure 4.

One of the advantages of the enhancement mode PHEMT is the ability to dc ground the source leads and still require only a single positive polarity power supply. Whereas a depletion mode PHEMT pulls maximum drain current when V_{gs} = 0 V, an enhancement mode PHEMT pulls nearly zero drain current when V_{gs} = 0 V. The gate must be made



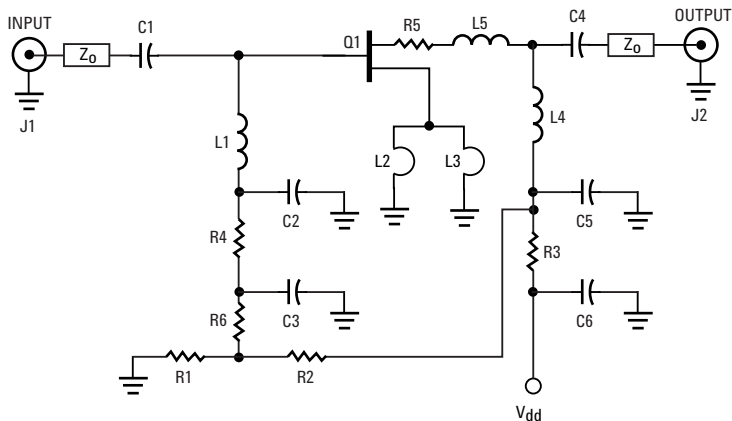


Figure 2. Schematic diagram of the low noise PCS amplifier using the ATF-55143.

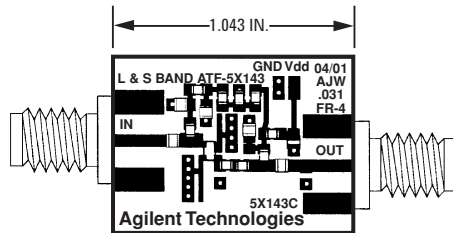


Figure 3. Component Placement Drawing for the ATF-55143 Low Noise Amplifier.

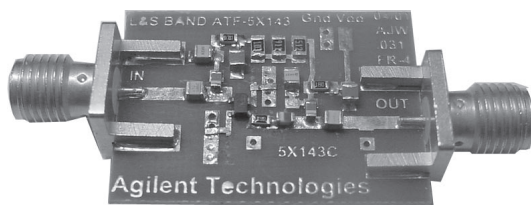


Figure 4. Photograph of completed ATF-55143 Low Noise Amplifier Demonstration Board.

positive with respect to the source for the enhancement mode PHEMT to begin pulling drain current. It is also important to note that if the gate terminal is left open circuited, the device will pull some amount of drain current due to leakage current creating a voltage differential between the gate and source terminals.

Biasing the ATF-55143 is accomplished by the use of a voltage divider consisting of R1 and R2. The voltage for the divider is derived from the drain voltage which provides a form of voltage feedback to help keep drain current constant. The purpose of R4 is to enhance the low frequency stability of the device by providing a resistive termination at low frequencies. Capacitor C3 provides a low frequency bypass for R4. Additional resistance in the form of R6 (approximately 10K Ω) is added to provide current limiting for the gate of enhancement mode devices such as the ATF-55143. This is especially important when the device is driven to P1dB or Psat.

The amplifier uses a high-pass impedance matching network for the input noise match. The high-pass network consists of a series capacitor (C1) and a shunt inductor (L1). The high-pass topology is especially well suited for PCS, W-CDMA and WLAN applications as it offers good low frequency gain reduction which can minimize the amplifier's susceptibility to cellular and pager transmitter overload. L1 also doubles as a means of inserting gate voltage for biasing up the PHEMT. This requires a good bypass capacitor in the form of C2. C1 also doubles as a dc block. The Q of L1 is ex-

Table 1. Component Parts List for the ATF-55143 Amplifier.

C1	5.6 pF chip capacitor
C2,C5	8.2 pF chip capacitor
C4	2.2 pF chip capacitor for best S_{22} and 5.6 pF for best OIP3 (see text)
C3, C6	10000 pF chip capacitor
J1, J2	SMA Connector, EFJohnson 142-0701-881
L1	2.7 nH inductor (Toko LL1608-FH2N7S)
L2, L3	Strap each source pad to the ground pad with .020" wide etch. The jumpered etch is placed a distance of 0.040" away from the point where each source lead contacts the source pad. Cut off unused source pad. See text
L4	10 nH inductor (Toko LL1608-FH10NK)
L5	5.6 nH inductor (Toko LL1608-FH5N6K)
Q1	Agilent Technologies ATF-55143 PHEMT
R1	910 Ω chip resistor
R2	4700 Ω chip resistor
R3	2.2 Ω chip resistor
R4	50 Ω chip resistor
R5	27 Ω chip resistor (see text)
R6	10K Ω chip resistor
Zo	50 Ω Microstripline

tremely important from the standpoint of circuit loss which will directly relate to noise figure. The Toko LL1608-F2N7S is a small multilayer chip inductor with a rated Q of 32 at 800 MHz. Lower element Qs may increase circuit noise figure and should be considered carefully. This network has been optimized primarily for noise figure with secondary emphasis on input return loss. A modest amount of source inductance in the form of L2 and L3 is used to improve input return loss with minimal effect on noise figure.

The amplifier uses a low-pass structure for the output impedance matching network. L5 and

C4 provide the optimum match for best output return loss coincident with good IP3. L4 is primarily an RF choke but its value can be critical to low frequency stability. L4 was chosen to be no greater than 10 nH to assist in lowering amplifier gain below 1.9 GHz. Suppressing amplifier gain below 1.9 GHz is critical from the standpoint of maintaining amplifier stability. Resistor R3 and capacitor C6 provide a low frequency resistive termination for the device which helps stability. C6 was chosen to be 10000 pF or 0.01 μ F over a 1000 pF capacitor in order to improve output intercept point slightly by terminating the low frequency (F2-F1) difference com-

ponent of the two test signals used to measure IP3. This can be especially important for the typical 1.25 MHz spacing used in CDMA IP3 evaluation.

One of the advantages of a narrower 400 micron gate width device such as the ATF-55143 is its increased gain. A drawback of increased gain can often be reduced stability. The ATF-55143 amplifier incorporates series resistive loading in the drain circuit in the form of R5. Without resistive loading the amplifier gain at 1960 MHz can be as high as 20 dB if the input and output matching networks are designed for best return loss. The amplifier will not be unconditionally stable under these conditions. The addition of R5 reduces amplifier gain both in-band and out-of-band which enhances stability. The resistive loading also allows for an increase in source inductance which can reduce in-band gain to an acceptable level.

Series resistive loading can quite often provide better broad-band stability as opposed to shunt resistive loading across L4. The reason for this can usually be attributed to circuit layout problems. If the stabilizing resistor is placed some electrical distance away from the drain, its effectiveness can be reduced. The phenomena is device and circuit layout dependent. The demonstration board is designed for use with any of the SOT-343 packaged family of Agilent Technologies enhancement mode PHEMT devices. The demonstration board was also designed so that the designer has several circuit options with which to optimize performance for a particular application. Component mounting pads are provided near

L4 to allow a resistor to be paralleled with L4 to lower gain and increase stability. Spaces are also provided for resistor R5 and inductor L5 to be inserted in series with the device drain lead. The space has already been jumpered on the demo board. Both jumpers will need to be removed with a sharp knife for the ATF-55143 amplifier design. It is important to remember that any amount of resistive loading in the drain circuit will effect gain and more importantly P1dB and OIP3. Resistor R5 lowers OIP3 by about 2 dB with the side benefit of increased stability.

Inductors L2 and L3 are actually very short transmission lines between each source lead and ground. The inductors act as series feedback to the device. The amount of series feedback has a dramatic effect on in-band and out-of-band gain, stability and input and output return loss. The amplifier demo board is designed such that the amount of source inductance is variable. Each source lead is connected to a microstripline which can be connected to a ground pad at any point along the line. For minimal inductance, the source lead pad would be connected to the ground pad with a very short piece of etch at the point closest to the device source lead.

A moderate amount of source inductance is used in the PCS amplifier design. Each source lead is connected to its corresponding ground pad at a distance of approximately 0.040" from the source lead. The 0.040" is measured from the edge of the source lead to the closest edge of the ground strap. See Figure 5. The ground straps are made from copper straps approximately 0.020" in

width. The straps are used to bridge the 0.020" gap from the source lead etch to the ground pad. The remaining unused source lead pad may be removed by cutting off the unused etch. On occasion, the unused etch which looks like an open circuited stub has caused high frequency oscillations. During the initial prototype stage, the amount of source inductance can be tuned to optimize performance. In the actual con-

version of the design to a board layout, each source lead etch can be made approximately .060" in length from the edge of the device source lead to the ground pad. The ground pad should have at least 2 plated through holes connecting the ground pad to the bottom ground-plane.

Performance of the ATF-55143 Amplifier

The amplifier is tested at a power supply voltage Vdd of 3 V which provides a device bias point of Vds = 2.7 V @ Id = 10 mA. The swept plots shown in Figures 6, 7, and 8 represent amplifier performance with the output coupling capacitor C4 at a value of 2.2 pF.

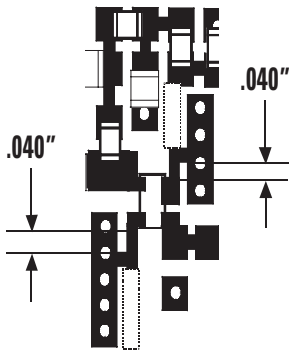


Figure 5. Source grounding for the ATF-55143.

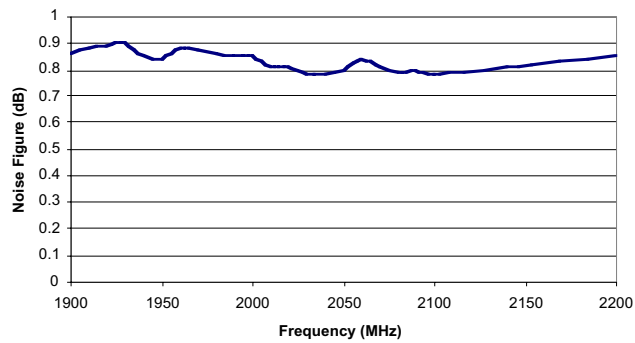


Figure 6. ATF-55143 Amplifier Noise Figure vs. Frequency.

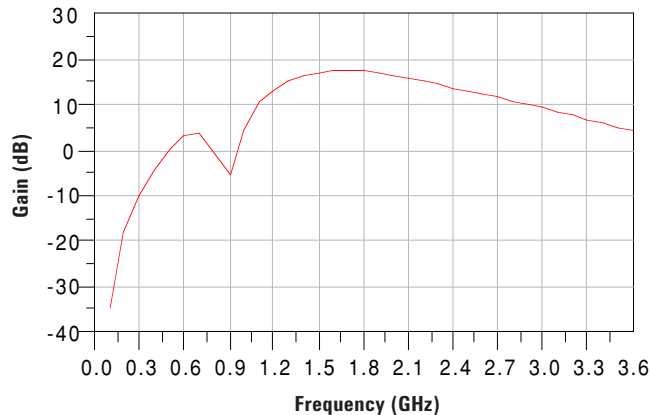


Figure 7. ATF-55143 Amplifier Gain vs. Frequency.

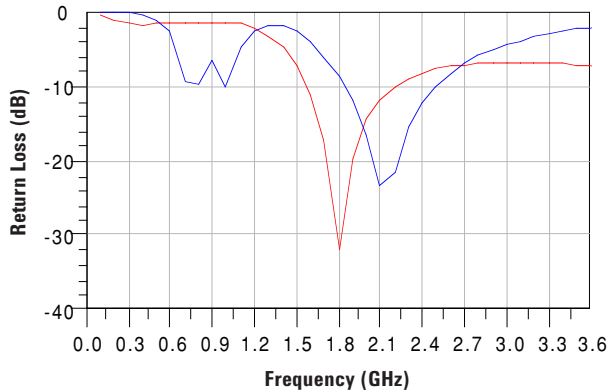


Figure 8. ATF-55143 Amplifier Input and Output Return Loss vs. Frequency

Table 2. Performance Comparison with Change in Value of Output Capacitor C4.

C4	1960 MHz Performance					2100 MHz Performance				
	S11	S22	S21	OIP3	IIP3	S11	S22	S21	OIP3	IIP3
2.2 pF	-17 dB	-15.5 dB	16.3 dB	+21.6 dBm	+5.3 dBm	-12.2 dB	-23.3 dB	15.7 dB	+22.9 dBm	+7.2 dBm
5.6 pF	-12.1 dB	-15 dB	16.3 dB	+22.8 dBm	+6.5 dBm	-9.9 dB	-13.5 dB	15.7 dB	+23.3 dBm	+7.6 dBm

The measured noise figure and gain of the completed amplifier is shown in Figures 6 and 7. Noise figure is less than 1 dB from 1900 MHz through 2200 MHz. Gain is approximately 16 dB at 1960 MHz and 15.5 dB at 2100 MHz.

Measured input and output return loss is shown in Figure 8. The input return loss measures a nominal -17 dB at 1960 MHz while the output return loss measured -15.5 dB. At 2100 MHz, the input return loss measures -12.2 dB while the output return loss measures -23 dB.

As with any amplifier, there is considerable interaction between input and output tuning. This generally occurs because the reverse isolation of the transistor (S12) is not zero. This causes interaction between input and output tuning. Tuning the input for best return loss may cause the output return loss to get worse. Generally the input circuit is tuned for best

noise figure with good return loss also being desired. The output circuit can then be tuned for best third order output intercept point (OIP3) which will not necessarily guarantee best output return loss. In addition, an output circuit tuned for best return loss will not always guarantee best third order output intercept point (OIP3).

The data shown in Table 2 summarizes the OIP3 performance with respect to input return loss (S11), output return loss (S22) and gain (S21). The standard LNA with C4 set to 2.2 pF yielded an OIP3 of +21.6 dBm with a corresponding input intercept point (IIP3) of +5.3 dBm at 1960 MHz. At 2100 MHz the OIP3 measures +22.9 dBm with a resultant IIP3 of +7.2 dBm. Changing C4 to 5.6 pF increased the OIP3 at 1960 MHz to +22.8 dBm with a resultant IIP3 of +6.5 dBm. The improvement in OIP3 at 1960 MHz comes with a slight degradation in input and output return loss.

Conclusion

The Agilent Technologies' ATF-55143 low noise enhancement mode PHEMT has been designed into a low noise amplifier application for both the PCS and W-CDMA markets. The amplifier provides low noise figure (0.9 dB) and very good IIP3 (greater than +5 dBm) coincident with good input and output return loss and approximately 16 dB gain at a bias point of $V_{ds} = 2.7$ V and $I_d = 10$ mA.

Appendix 1. Determining the optimum amount of source inductance

Adding additional source inductance has the positive effect of improving input return loss and low frequency stability. A potential down-side is reduced low frequency gain, however, decreased gain also correlates to higher input intercept point. The question then becomes how much source inductance can one add before one has gone too far?

For an amplifier operating in the 2 GHz frequency range, excessive source inductance will usually manifest itself in the form of a gain peak above 6 GHz and even sometimes above 12 GHz. Normally the high frequency amplifier gain roll-off will be gradual and smooth. Adding source inductance begins to add bumps or gain peaks to the once smooth gain roll-off. The source inductance while having a degenerative effect at low frequencies is having a regenerative effect at higher frequencies. This shows up as a very high frequency gain peak (S21) and also shows up as input return loss (S11) becoming more positive. Some shift in upper frequency performance is OK as long as the amount of source inductance is fixed and has some margin in the design so as to account for S21 variations in the device.

A wide-band gain plot of S21 for an amplifier using the 400 micron gate width ATF-55143 device is shown in Figure 1. The plot shown in Figure 1 represents an amplifier that uses minimal source inductance and has a relatively flat gain response at the

higher frequencies. The amplifier has relatively high gain at 2 GHz but less than 0 dB gain above 6 GHz.

The wideband gain plot shown in Figure 2 is for the same amplifier that uses additional source inductance. Increased source inductance improves low frequency stability by lowering gain at 2 GHz. Input return loss will also be improved while noise figure will stay relatively constant. The effect of adding additional source inductance can be seen as some gain peaking above 6 GHz. This level of gain peaking shown in Figure 2 is not considered a problem because of its relatively low level compared to the in-band gain.

Excessive source inductance will cause gain to peak at the higher frequencies and may even cause the input and output return loss to be positive. Adding excessive source inductance will most likely generate a gain peak in the 12 to 13 GHz frequency range which could approach several dB. Its effect can be seen in Figure 3. The end result is poor amplifier stability especially when the amplifier is placed in a housing with walls and a cover. Larger gate width devices such as the 800 micron ATF-54143 will be less sensitive to source inductance than the smaller gate width devices and can therefore tolerate more source inductance before instabilities occur. The drawback of the ATF-54143 will be reduced gain. The wide-band gain plot

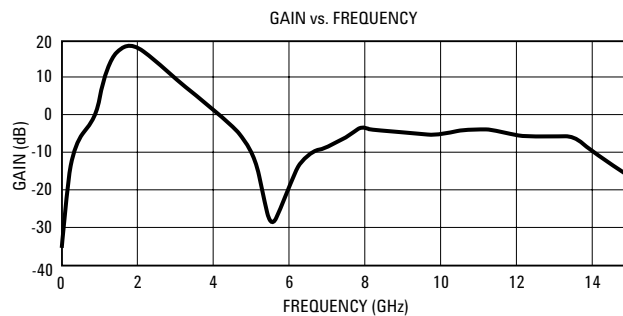


Figure 1. Wide-band gain plot of 2 GHz ATF-55143 amplifier using minimal source inductance.

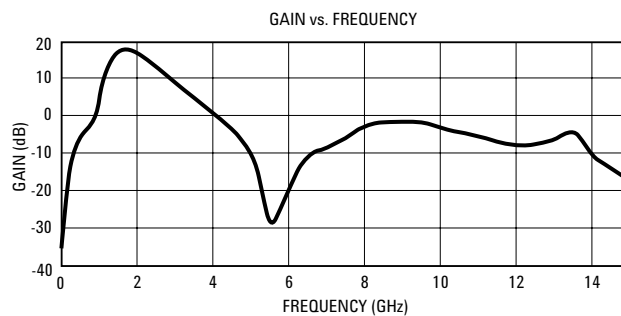


Figure 2. Wide-band gain plot of 2 GHz ATF-55143 amplifier with an acceptable amount of source inductance.

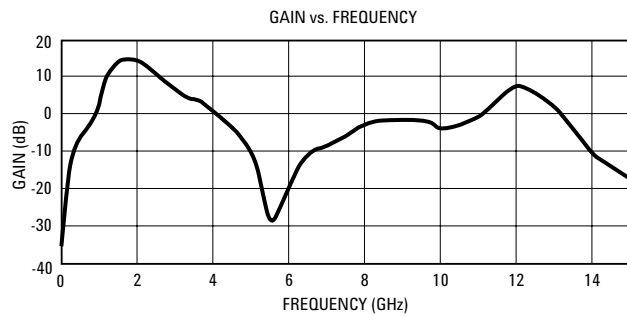


Figure 3. Wide-band gain plot of 2 GHz ATF-55143 amplifier with an unacceptable amount of source inductance producing undesirable gain peaking in the 12 to 13 GHz frequency range.

does give the designer a good overall picture as to what to look for when analyzing the effect of excessive source inductance.

Circuit topology can also effect high frequency gain and its resultant effect on high frequency stability. The low pass network topology as used in the output of the 2 GHz ATF-55143 amplifier was found to decrease high frequency gain and therefore improve amplifier stability at higher frequencies.

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